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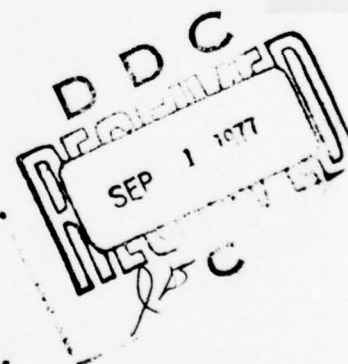
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SYNCHRONOUS METEOROLOGICAL SATELLITE DIRECT READOUT GROUND SYSTEM DIGITAL VIDEO ELECTRONICS

By
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Atmospheric Sciences Laboratory

US Army Electronics Command
White Sands Missile Range, New Mexico 88002

June 1977

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ERRATA PAGE FOR ECOM-5825

SYNCHRONOUS METEOROLOGICAL
SATELLITE DIRECT READOUT GROUND
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Page 9, third paragraph on page, first and second lines in paragraph

Change "Another area that has required hardware redesign in the location of the grid bit is the IR data word." to "Another area that has required hardware redesign is the location of the grid bit in the IR data word."

Page 9, sixth paragraph on page, second line in paragraph

Change "This switch in the program mode G sets..." to "This switch in the program mode sets..."

Page 10, changes:

second paragraph, second line: Change Schematic AZA5 to Schematic A2A5

third paragraph, first line: Change Schematic AZA5 to Schematic A2A5

third paragraph, fifth line: Change Schematic AZA2 to Schematic A2A2

third paragraph, eleventh line: Change Schematic AZA12 to A2A12

third paragraph, twelfth line: Change "B AZAZ pin 29..." to "B A2A2 pin 29..."

fifth paragraph, fourth line: Change AZA5Z24 to A2A5A24

fifth paragraph, fifth line: Change A3A5 A3Z to A3A5 A32

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The material presented in this report is a brief introduction to the Synchronous Meteorological Satellite (SMS) stretched Visual and Infrared Spin Scan Radiometer (VISSR) data down link. A brief description of the Direct Readout Ground Station (DRGS) follows. This is intended to give the reader a very general concept of the VISSR signal origin and user termination. Problem areas in the White Sands Missile Range DRGS are pointed out, and steps taken to correct the problems are briefly explained. The White Sands Digital			

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20. ABSTRACT (cont)

Video Drawer is explained in great detail. Schematics are provided to help the reader through the explanation. The digital video drawer is the heart of the analog processing system and has presented the most problems.

This report will be followed by additional reports and future updates and subsystem components.

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INTRODUCTION

The Synchronous Meteorological Satellite (SMS) program originated in March 1974 with the launch of the SMS-A. The White Sands Missile Range (WSMR) Direct Readout Ground Station (DRGS) was delivered in the same month and received the first picture transmitted from the satellite on 25 May 1974.

Operational experience and consultation with researchers requiring SMS data revealed the need to refine the basic DRGS and to add the data processing equipment necessary to fully exploit the information contained in the SMS data stream. The research groups require data files which are computer compatible, sectorized to a specified area, and highly reliable in terms of low error rates. Hard copy film images are required on a daily basis to allow selection of areas which might be of interest for intensified study.

This report describes some of the steps taken to upgrade the original system.

BACKGROUND

The SMS views the earth from a nominal altitude of 22,300 miles. The satellite receives its operational commands from the Command Data and Acquisition (CDA) Station at Wallops Island, VA. In its normal operational mode, it is commanded to transmit its data once each half hour.

The satellite has a nominal rotation speed of 100 rpm. This rotation generates the West-East scan of the earth. At the nominal 100 rpm rate, the period of scan is 600 msec.

To generate the North-South earth limits, a stepper mirror is incorporated. One thousand eight hundred and twenty-one steps of this mirror generated the North-South satellite earth viewing window. Each step is about 4 miles.

The data collection sensors consist of eight visible and one infrared (IR). A second IR sensor is available as a backup. The nominal resolution of each visual sensor is 1/2 by 1/2 mile. The 2- by 4-mile resolution for the IR sensor generates the IR data for the same area.

In one revolution of the satellite, the earth is scanned for about 18 degrees. Each scan consists of data from one IR sensor and eight visual sensors. These data are transmitted to the CDA station at a 28-megabit rate. The data are time stretched to fill the remaining 342 degrees of satellite rotation and retransmitted back to the satellite. The satellite retransmits the data back to earth where it is available to the users at a 2-megabit data rate.

The above explanation deals with the mode A data transmission (Fig. 1). The other modes, B and C/D, are shown in Fig. 1 also. The general operation is the same except the visual sensor data is averaged in operating modes B and C/D as shown in Fig. 1.

Except for the initial satellite checkout phase, modes B and C/D have never been used; therefore, the remaining discussion will deal with mode A operation only.

The stretched VISSR data is received at the users ground station, DRGS, at about 1687.1 MHz.

DIRECT READOUT GROUND STATION

The DRGS receives the 1687.1 MHz signal via a 25-foot parabolic dish antenna. Here the signal is amplified, down converted, and transmitted through semirigid coax to the receiver at 137 MHz.

The block diagram in Fig. 2 shows the signal flow. The 137 MHz receiver amplifier filters and generates a final intermediate frequency of 10 MHz which is routed to the phase shift keyed (PSK) demodulator. Here the 10 MHz carrier is stripped off and the data are sent to the bit and frame synchronizers. The bit synchronizers provide a 0° and 90-degree phase clock to the frame synchronizer. The frame synchronizer decides which data is being processed (IR or visible) and generates line syncs, word counts, step commands and serial to parallel data conversion.

The data enters the digital video electronics drawer in a parallel word format. This unit is the heart of the data handling capabilities for the laser beam recorder (LBR). It contains the logic required for data enhancement, memory control, and data transfer decision network.

In addition to the data control logic, the drawer also includes a digital to analog converter (DAC) to drive the laser beam modulator driver. The data presented to the DAC must pass through 1 of 16 lookup tables. These lookup tables provide the enhancement capabilities for real-time LBR transparencies.

The modulator driver modulates the laser beam as it passes through a liquid crystal. Lenses and mirrors pass the light beam to the stepper motor optics. The rotating drum that holds the film rotates in synchronism with the satellite, and the stepper motor transverses across the film at the transmitted line rate. The drum rotation gives the West-East earth coverage and the stepper motor generates the North-South earth coverage. The nominal 1821 steps of the satellite mirror take 18.2 minutes to complete the full earth coverage. Processing of the film adds another 3 minutes.

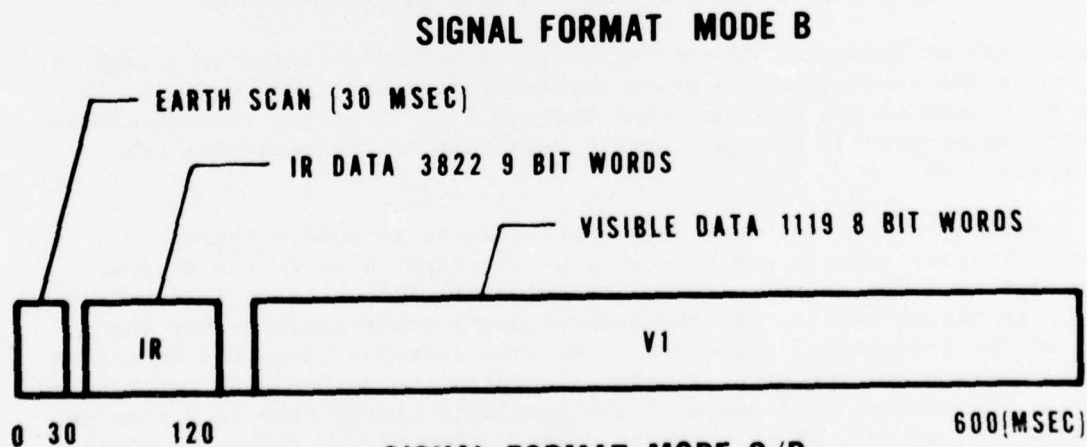
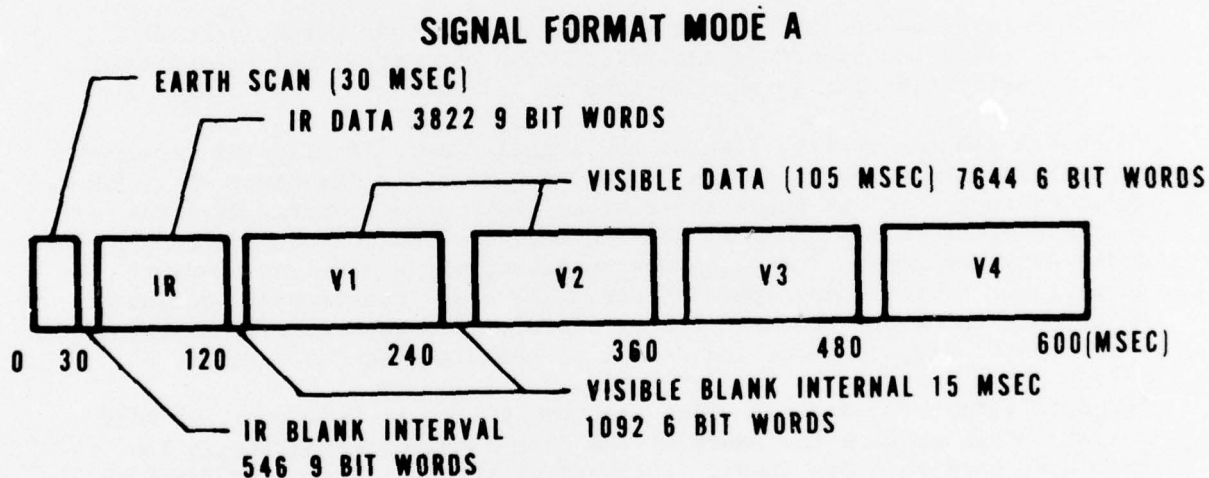
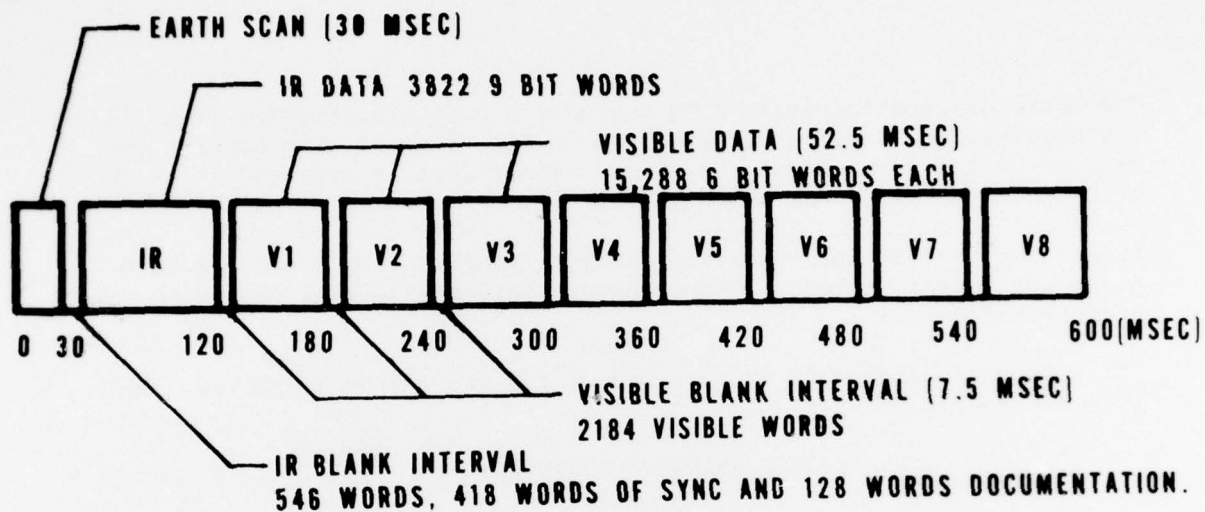
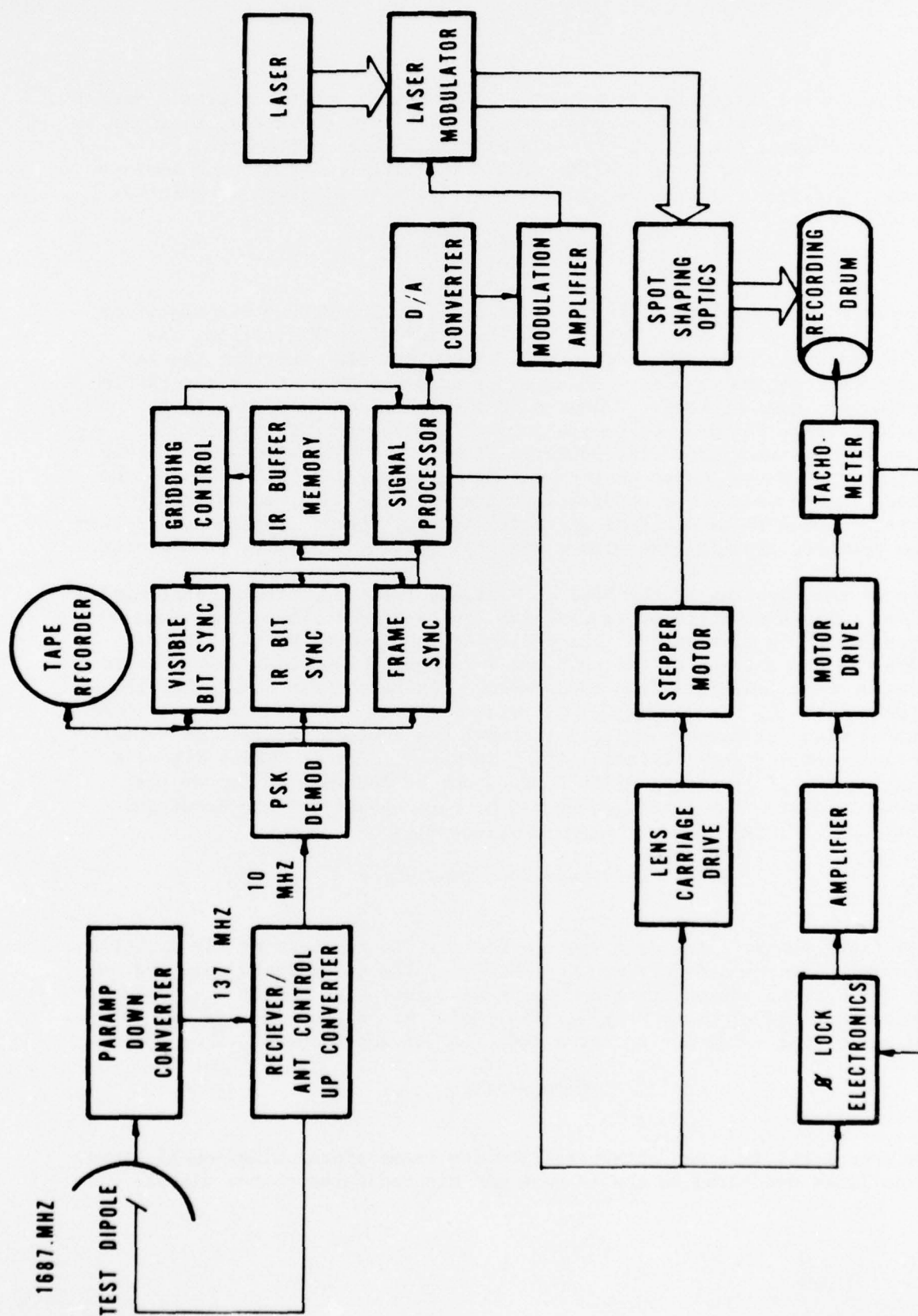


FIGURE 1 DATA TRANSMISSION FORMATS



Modifications

The following discussion is a detailed explanation of the system's operation and problem areas. The antenna system, down converter, receiver, and demodulator subunits have required very little maintenance or redesign. These units are quite similar to most receiving type equipment; therefore, a detailed explanation of their operation is omitted.

Front End

The front end consists of the antenna, a filter, a parametric amplifier, phase lock source, and a mixer. In the original configuration, the phase lock source would lose lock. Temperature and vibration checks produced negative results, and no other cause could be found for the intermittent loss of lock. Redesign of the front-end component layout to facilitate retuning of the phase lock source without removing it from the system reduced the downtime from 1 day to 30 minutes. Another supplier of phase locked sources was established, and the design of the phase locked source was changed from the existing external reference crystal model to an internal reference crystal model. This configuration has operated trouble free with a mean time between failures of 8 months.

Due to the location of the DRGS on WSMR and its associated missile mission, a large quantity of radiosondes are launched. These radiosondes operate in the same band as the SMS down link frequency, the S-band. Although the antenna of the DRGS has a 2-degree beam width which should provide some isolation from interference, operation has shown that the signal strength of radiosondes is enough to cause interference. Coordination with our meteorological personnel has reduced the rate of interference but has not eliminated it. The design of radiosondes allows a high degree of frequency drift that cannot be compensated for at the present time. This interference may be causing some of the front end downtime, but this has not been confirmed yet.

Bit and Frame Synchronization

The frame synchronizer is a special design. To the best of the author's knowledge, there are only two in existence, the White Sands unit and one in the National Aeronautics and Space Administration Mobile Van System. These units have yet to be fully analyzed. Minor changes have been made, mainly signal conditioning and a reduction of input/output (I/O) cables.

Changes Made

Word parallel data was outputted from the frame synchronizer on 15 lines. Nine lines dedicated to the IR data and six dedicated to the visible.

Since the data are transmitted time multiplexed, there is no rationale for separate lines for each set of data. Therefore, the data was shared on the I/O nine IR lines. This eliminated six I/O lines.

All data exit the frame synchronizer on single-ended lines, driven by standard transistor-transistor logic gates; these were placed with line driver/receiver pairs for differential drive data output. The same procedure was followed with the input clock and other timing signals.

The results of these changes completely eliminated all cross talk and other interference on the frame synchronizer output lines.

Changes to be Made

The SMS data stream contains documentation data at the beginning of each line. These documentation data give information about the satellite orbit configuration. In the present system these data are blocked. For a system that is dedicated to transparency generation this is a logical approach, but for computer analysis of the digital data the documentation data contain useful information.

The frame synchronizer contains word count counters that serve no purpose at present. The logic chips have been removed, but the back plane wiring is still intact. If a word counter is necessary it should be in the unit that requires the counter, eliminating the 14 output cables required for the word count output.

Digital Video Drawer

This drawer is the heart of the LBR data formatter. Data enters in a word parallel format along with word clocks, line syncs and step command. IR storage, grid bit extraction logic, lookup tables, and DAC take place in the unit. Since the unit is the major data handling subunit and one of the more complex subunits in the system, it was a major problem area.

Figure 3 shows a block diagram of the digital video drawer. Data enters this unit from the frame synchronizer. It is held in an input buffer until clocked out by the proper word clock; then it enters the read/write memory. This memory is a 4K by 18 bit stack, horizontally split to provide two 4K by 9 bit sections. The first 4K by 9 bit section provides buffering of the IR data; the second section is used as a lookup memory to provide film gamma correction and various preprogrammed enhancement curves. The memory has the capacity to store up to 16 sets of curves for gamma correction or enhancement.

For gridding and IR data processing, the IR data must be buffered. IR data is routed to half of the 4K by 9 bit memory and then recirculated

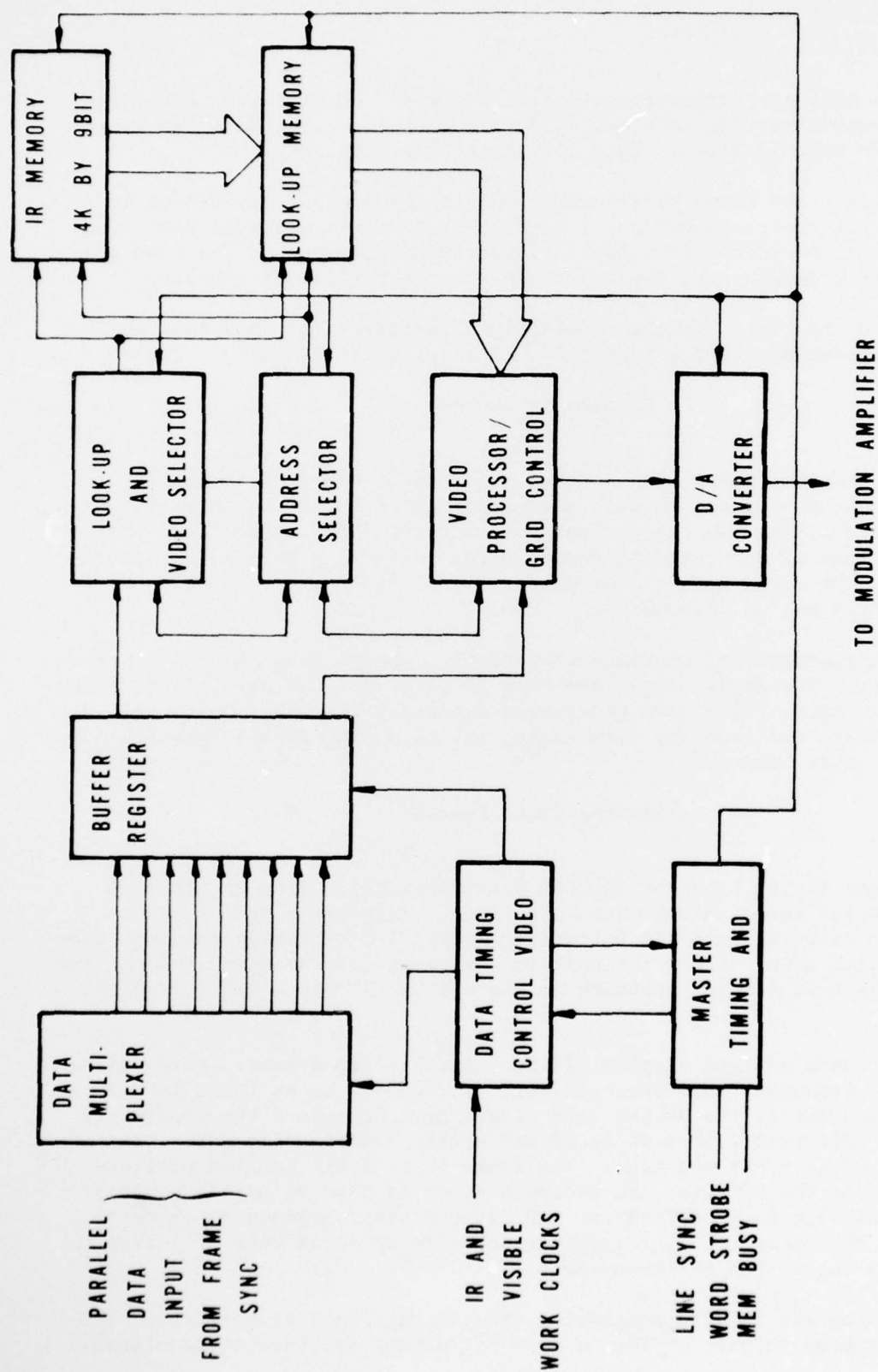


FIGURE 3 DIGITAL VIDEO DRAWER BLOCK DIAGRAM

eight times to the DAC. The recirculation is synchronous with the visible time interval such that the IR data is processed during visible time. The grid bit is the most significant bit (MSB) of the 9 bit IR data word. Grid bit data is used to cause the video to be white or black as determined by the video level. To obtain this output, the IR and visible must be compared at all points along the scan line. As the IR and visible data points are compared synchronously, the time of occurrence of the grid point is determined. This point is compared to the intensity value of the visible data at that time and a white or black data value is substituted for it. The transfer signal that commands the buffer to transfer its stored data to the DAC originates from the memory timing circuitry.

Modification to the Digital Video Drawer

This subunit has been completely redesigned. The components and theory from the original design were used, but their logic and layout were replaced. The original documentation for their unit was erroneous and incomplete. Many of the components in this drawer were unused. As a result of the redesign, troubleshooting time has been cut in half. In one case six boards containing an average of 26 chips per board were replaced by one printed circuit board containing 20 chips.

Another area that has required hardware redesign in the location of the grid bit is the IR data word. The gridding information is contained in the MSB of the IR word, which means that the sensor data information of the IR and visual word are displaced by one bit. When the serial data stream is shifted into a parallel data word, the MSB of the IR word is the grid bit with the MSB of the visible word being sensor data. To align the data, the visible parallel word must be shifted one bit position to align sensor data information.

This misalignment of sensor data would not have occurred if the gridding information had been in the least significant bit location of the IR word. Then the MSB of the IR sensor word and the MSB of the visible sensor word would have been in alignment.

The following is the theory of operation of the digital video drawer.

PROGRAMMING

Programming of the lookup tables is initiated by the front panel program run switch. This switch in the program mode G sets the Q output of Z9 (pin 5) and locks the memory to mode 2 which is the lookup table portion of the memory. The mode control lines split the core into two 4K by 9 bit sections. Mode 1 is the IR data storage section. The anded signal of the front panel program switch and the Q output of Z9 lock out mode 1 during program time.

The core address switches also function as data entry switches. In mode 1, four address lines are tied to front panel switches which split the mode 1 or lookup section of the memory into sixteen sections. Each section is 9 bit by 256 locations. This leaves eight switches for addressing and data entering.

The program/run switch also blocks the input word rate clock by putting a low on pins 2 and 13 of A22 Schematic AZA5. The lookup section to be programmed is selected by the four front panel switches with the other eight in the zero position. This selects the starting address location when the examine switch on the memory control is pressed.

The examine switch Schematic AZA5 sets the Q output of A24B high. This switch is a momentary switch and the Q output of A24B goes low when it is released. This generates an input data strobe. The write operation is inhibited at this time so that the data stored in this location can be examined. The input data strobe clocks Z8 Schematic AZA2 which generates memory initiate through Z14 pin 4. At the end of memory busy Z1 triggers, which resets Z8 pin 9 through Z8 pin 6 and generates a second memory initiate. The second memory busy cannot generate another memory initiate because Z14 pin 1 is high. The first memory initiate sets Z7 and 9 such that address select A selects the address counter for the memory address (J6-54, J5-54, J4-54, Schematic AZA12). Address select B AZAZ pin 29 is zero when in the program mode.

Lookup (LU) select A A2A2 pin 9 initially allows the LU lines to address the memory. The first memory initiate puts a "zero" on LU select A and a "one" on LU select B. This in conjunction with the address select lines places the address register on the address lines of the core. The second memory initiate switches the LU lines to the address lines and allows the data stored in the address location to be examined.

When a word is to be programmed, the signal flow is similar to the examine routine. The main difference is that the write inhibit is generated and the programmed data value is stored in the memory. The momentary enter switch toggles, which sets the Q output of AZA5Z24 pin 5. This generates an input data strobe through A3A5 A3Z and a write inhibit through A2A5A23. When the switch is released A2A5A24 pin 5 returns to the reset state. With the front panel data switches set to the desired value, the input data buffers pass the data values to the holding registers A2A5A30 and A31. The data is clocked into the registers by the trailing edge of the input data strobe.

With the this/next switch in the "this" position, the memory address register is held in the address previously selected and the data will be stored in that address. With the switch in the "next" position, the memory address register is allowed to autoincrement and the data is then stored in the next address location.

RUN MODE

In the run mode, timing is initiated from the frame synchronizer. IR sync clocks A2A2 Z9 pin 5 high via the line receiver, which puts a low on the mode 1 (IR storage) control of the memory and allows the IR data to be written and stored in memory. Mode 2 control is maintained in the high state while in the run mode. Therefore, data can never be written into the LU tables while in the run mode. IR data clocks are gated through A2A5A22 to generate the input data strobe. The input selector selects the IR lines at input. These data are clocked into the buffer register by the trailing edge of the input data strobe. The trailing edge also generates a memory initiate pulse via Z8 and Z14 of the A2A2 card. The remaining sequence is the same as the program cycle. Upon completion of the IR cycle, visual sync resets Z9 via the line receiver and Z12 pin 8. Mode 1 control and mode 2 control of the memory are now in a read only state. Visible data clocks are gated through A2A5A22 to generate the input data strobe and select the visible data lines as input to the buffer registers A30 and A31. Address select A and B select the lookup lines as input to the memory's address. Lookup select A and B select the data lines to be present on the lookup lines.

Therefore, the visible data selects an address on the first cycle of the memory. The end of memory busy of cycle 1 generates cycle 2 memory initiate. Now the lookup select A and B passes the data that is stored in the memory location selected. This data, i.e., the programmed lookup word, is then present on the buffer register of the DAC. These data are clocked into the register by the video latch data strobe (pin 31 of A2A2).

The video latch data strobe is generated by the end of cycle 2 memory busy. Cycle 2 memory busy fires A2A2Z1 pin 10 on its trailing edge. One hundred nanoseconds later Z3, a 400 nsec one-shot, is fired via pin 2. Z14 pin 1 has gone high because the end of cycle 1 memory busy triggered Z8 pin 3 and reset Z8 pin 13. This inhibits a memory initiate pulse from being generated at the end of the input data strobe and clocks Z7 pin 11 to put a high on address select A and sets the lookup select signals to the proper states. At the end of cycle 2 memory busy Z7 pin 11 gets clocked by the Z3 pin 4 one-shot and the fall of the signal on Z7 pin 9 fires the video latch data strobe one-shot Z3 pin 10. The data are latched into the DAC buffer register A2A8 at this time.

This completes a cycle of visible data; i.e., the only data available to the DAC is visible. If the operator selects IR data to be available at the DAC, the sequence is similar because the IR data is inserted in the visible time interval. When IR data is selected on the front panel, pin 35 of A2A2 goes low.

IR data is written in memory as explained above. During the visible interval, lookup select B is held in the high state. Thus during the visible time interval the LU line selector looks at the IR data stored in memory and at the data lines which have the visible data present on them.

IR DATA OUTPUT THEORY

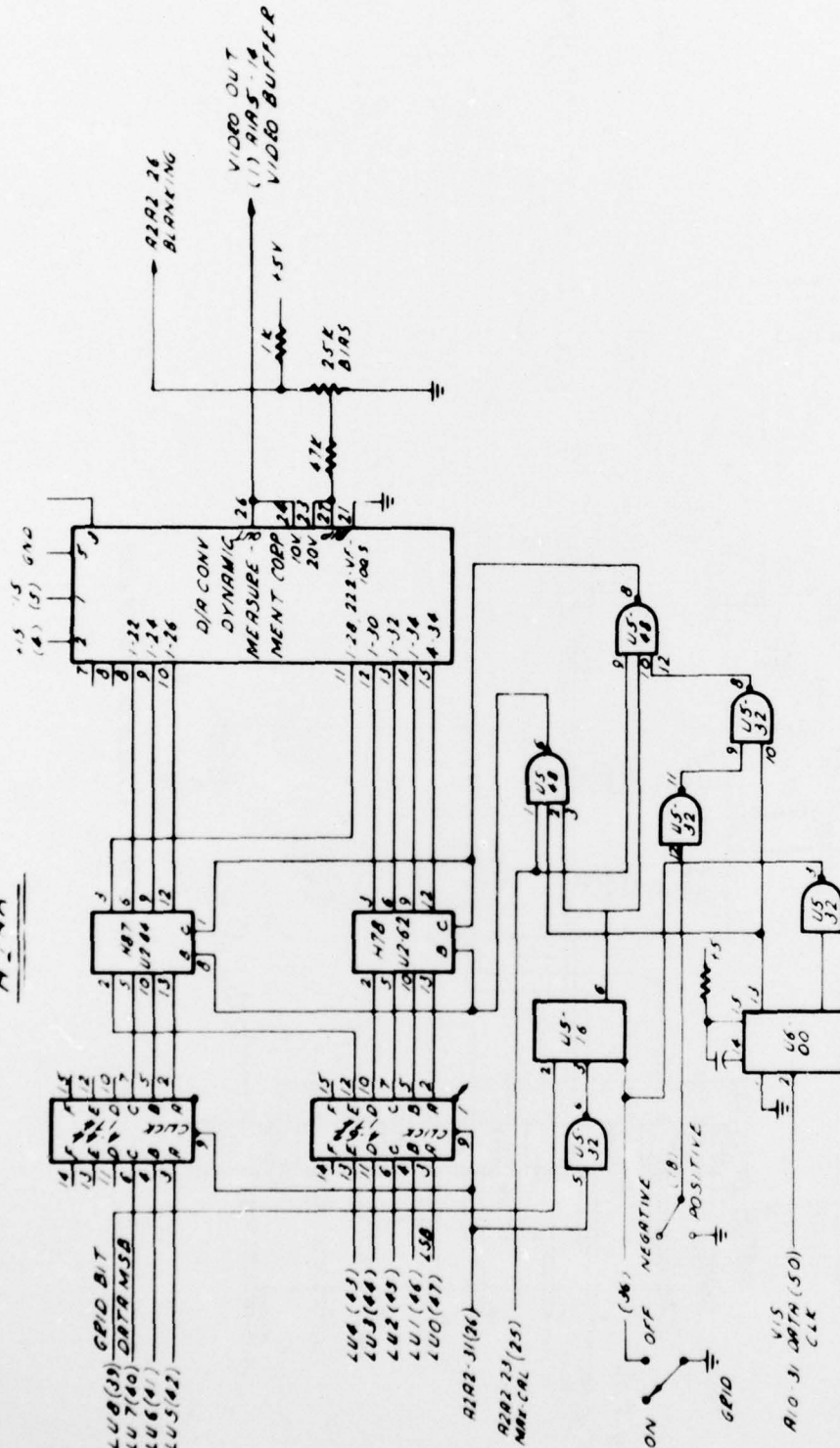
At the end of the IR interval, visible sync resets Z9 via the line receiver and Z12 pin 8 of A2A2. The mode 1 and 2 read/write controls of the memory are now in the read only state. Visible data clocks are gated through A2A5A22 to generate the input data strobe and select the visible data lines as input to the buffer register. These data are present on the "D" lines of the lookup line selector (1 out of 4 decoder A2A10). Since the lookup select B signal is held in the high state, the selector selects the memory lines as input with lookup select A low. A2A2 Z7 pin 9 is initially low; therefore, address select A is low with address select B in the high state during the visible time interval the address selector selects the 4 address registers as its input. The input data strobe generated by the visible word rate clock clocks the master address registers A2A12J3, 4, 5, and 6. The fourth clock from this register is the input clock to the 4 address register. This allows every fourth visible word rate clock to read a new IR word from memory. Each IR word is cycled four times before it is updated; i.e., $15,288 \text{ visible words} / 3,822 \text{ IR words} = 4/1 \text{ ratio}$. This technique mates the IR and visible display formats for the laser beam recorder.

The input data strobe generates the first memory initiated pulse by clocking Z8 pin 11 of A2A2. Z8 pin 8 goes low, which fires the 100 nsec one-shot Z14 pin 1. Z8 pin 9 puts a high on Z7 pin 12. Address select A is low with address select B remaining high during the full visible time interval. This sets the address selectors A2A12J5 and J6 to select the 4 address register as its input. The memory initiate pulse reads the first IR word out of memory. The address selector must now be changed to accept the LU lines as its input and the lookup selector must look at the IR data word before the next memory initiate is generated. Four hundred nanoseconds after the input data strobes trailing edge, the address select A flip-flop Z7 pin 11 gets clocked by Z3 pin 4. Address select A goes high and lookup select A pin 9 of A2A2 goes high. Lookup select B remains high during the IR selection time by the low on Z7 pin 2. Z7 pin 2 is held low by the front panel data selection switch in the IR mode. Therefore, address select A is high, address select B is high, lookup select A is low with lookup select B high. With these conditions, the lookup selection selects the IR data to be available on the lookup lines and the address selection selects the lookup lines on the address to the memory.

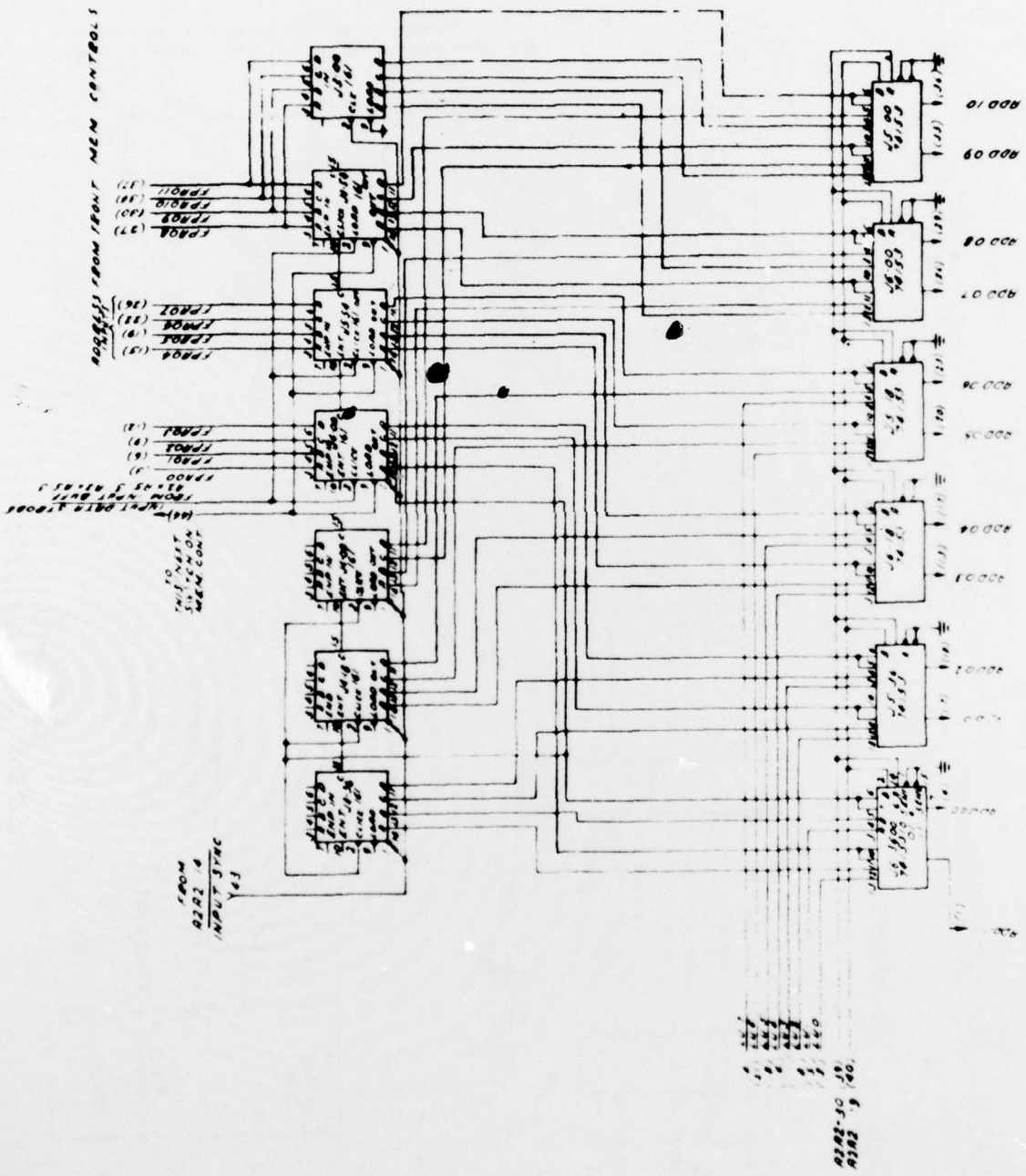
Cycle 1 is now completing its phase and the end of cycle 1 memory busy generates cycle 2. Cycle 1 memory busy fires Z1 pin 10 of A2A2. This 100 nsec pulse again fires the 400 nsec one-shot Z3 pin 2, fires the memory initiate one-shot Z14 pin 2, and clocks Z8 pin 3. Z8 pin 3 clocks and pin 6 goes low resetting Z8 pin 13. The Q output of Z8 places a high on Z3 pin 1 which will block the cycle 2 memory busy. A14 pin 1 is also high and will not pass the 100 nsec pulse generated by the end of cycle 2 memory busy. Cycle 2 memory initiate reads the lookup word out of memory, and this value is now available on the lookup program lines of the lookup selector.

The lookup selector must now make this data available on the lookup lines. Three hundred nanoseconds after cycle 2 memory initiates, Z3 pin 4 goes high clocking Z7 pin 11, putting a low on address select A. When lookup select A went high, Z3 pin 10, the data latch one-shot, clocked. These data are latched into the digital to analog buffer register 1.6 nsec later, after the programmed lookup word is available on the lookup line.

A22A



A22A
DIGITAL TO ANALOG CONVERTER



A2A12
ADDRESS REGISTER

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2. Westinghouse Electronics Corporation "Direct Readout Ground Station," Equipment Manual for the White Sands Missile Range System.

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